IN THE ABSTRACT:

Please replace the Abstract with the following:

A semiconductor device includes a memory cell array, latch circuits, first to third circuits and a current control circuit. The memory cell array includes NAND cells arranged therein. The latch circuits temporarily hold data read out from the memory cell array. The first circuit generates a first current varying in proportion to "1" or "0" of binary logic data of one end of the plurality of latch circuits. The second circuit generates a second current which is preset. The third circuit compares the first current with the second current. The value of "1" or "0" of binary logic data of the one end of the plurality of latch circuits is detected based on a result of the comparison between the first current and the second current.